FE-I Run Status and Next Steps

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Status of IBM Engineering Run for FE-I

- Reticle and DRC waivers accepted by IBM on Nov 20
- Wafer layout error noticed on Nov 27, causing some delays
- Expect more detailed information on wafer map and production schedule this week

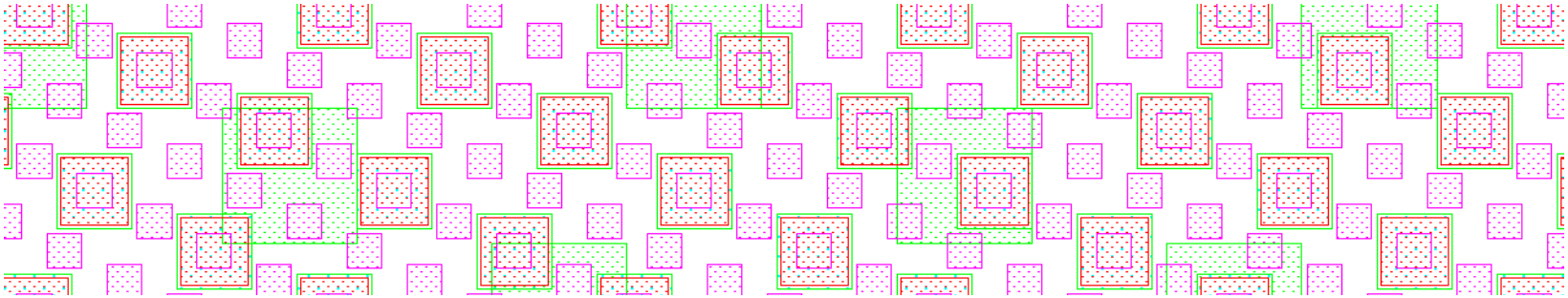
Next steps for wrapping-up FE-I1 design

- Complete HSPICE simulations for FE
- Complete TimeMill/PowerMill simulations for digital readout
- Begin work on front-end design improvements for FE-I2

Status of FE-I Engineering Run

Reticle and DRC Waivers accepted by IBM:

- Only one DRC error that we were required to fix (IBM did not accept our waiver request). This was in Analog Test chip, and was a violation of TV opening space rules in a capacitor array. The openings were removed, causing one day of delay.
- We received back the filled IBM GDS file (118 MB), and it looks correct. Fill was excluded over complete FE-I chips, DORIC preamp, CapTest chip, and Alignment Marks. Filling is generally large numbers of 1μ, 2μ, and 4μ squares:



- CERN discovered IBM error in wafer map layout on Nov 27. Had switched the locations of “thin” and “fat” test structures, making dicing of FE-I to correct size very difficult. They are now re-doing this, but it will cause some delay in wafer delivery.
- PO for additional 6 wafers now complete. Expect delivery of additional wafers within several weeks of initial run (or possibly even at the same time).
- No firm delivery date, but last half of January seems most likely. Should get more detailed information, along with final wafer map, soon. This will allow starting on bumping masks, as well as finalizing chip labeling and probing software.

Reticle for FE-I Run

All designs use same pads, and have logo for identification.

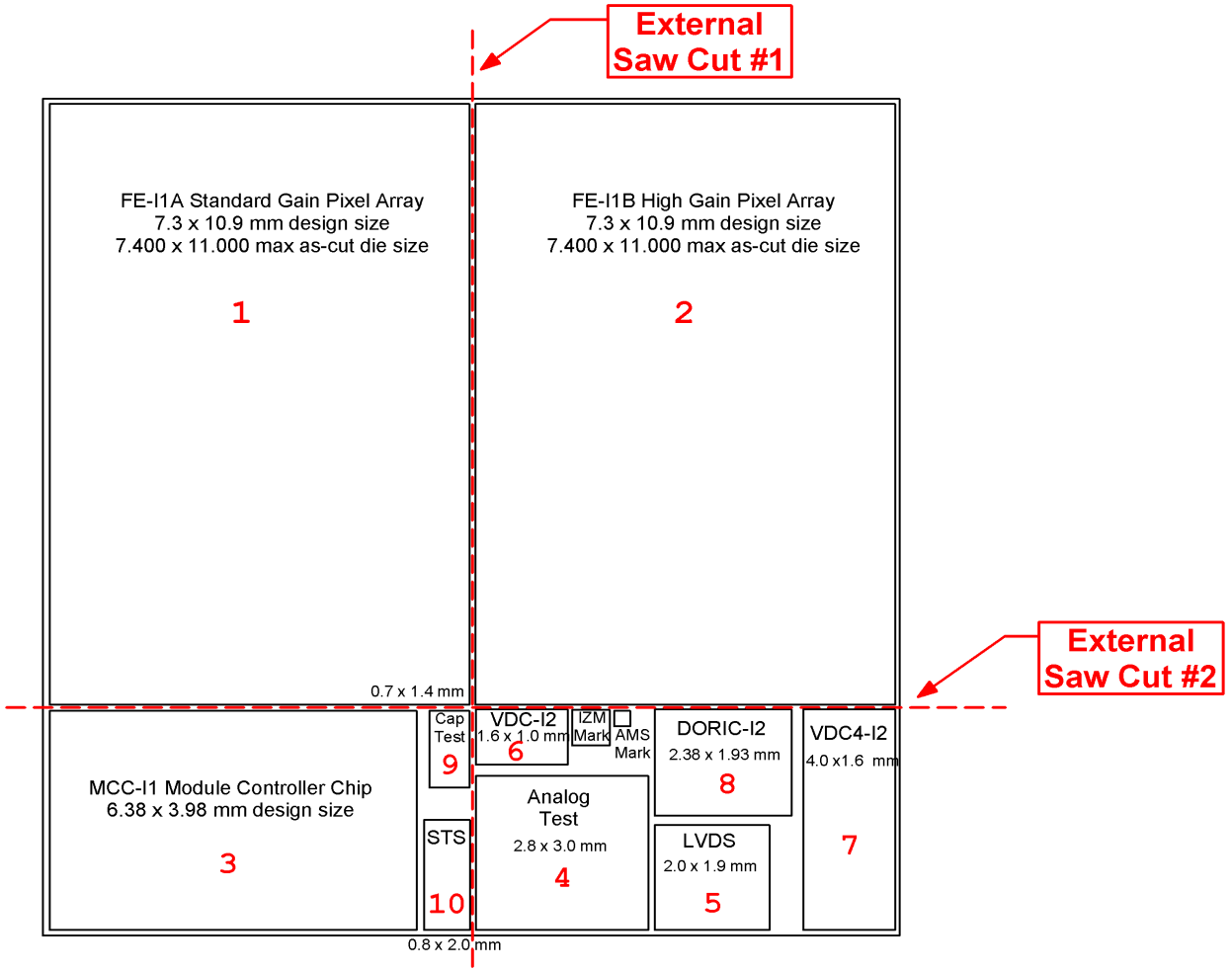
- **Two FE-I chips:** the left one is FE-I1A (10fF) and the right one is FE-I1B (5fF).
- **MCC-I chip:** this is the complete new MCC with U-pinout to satisfy module constraints.
- **DORIC-I and VDC-I chips:** they are improved versions of the designs submitted in the Feb MPW run, including 4-channel VDC. These are the “I2” generation.
- **Analog Test Chip:** this is very similar to the test chips fabricated in Feb/Mar with IBM and TSMC, but contains the final design and layout of all analog blocks, and 56 pixels instead of 20 (28 of each of the two types from FE-I)
- **LVDS Buffer Chip:** this is a convenient way to include the interface between a single chip and our test system into a rad-hard chip. It contains 4 LVDS->CMOS converters, 3 LVDS->LVDS repeaters (3.5mA outputs).
- **CapTest Chip:** this uses the CapMeasure circuit to provide characterization of all M1, M2, and M3 parasitics using a total of 64 test structures.
- **PM bar:** may be useful for checking details of device characteristics, although the very good parameter stability seen so far suggests it may no longer be needed. We have taken the CERN test structure and converted it to a 5-metal layout.
- **Alignment marks:** we have included the structure requested by Alenia and the one requested by IZM. These are for alignment of the wafer-scale bump masks.

Final reticle layout:

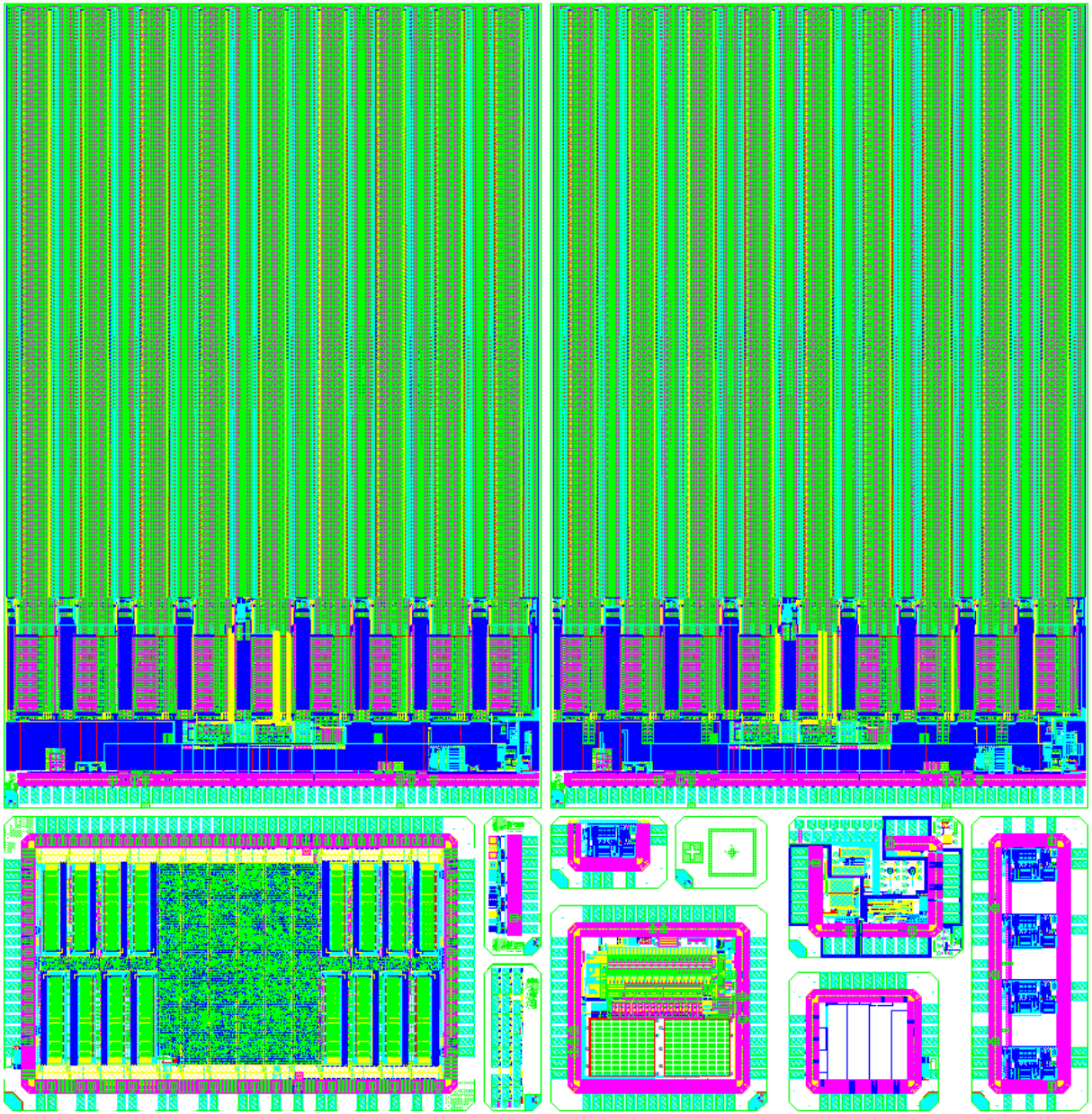
Reticle size is: 14.700 (W) x 15.000 (L) mm.

**IBM adds 138μ in one direction and 378μ in the other direction.
We choose to have the 138μ added to the left/right of the reticle shown here,
and to have the 378m added above/below the reticle shown here. This allows us to meet
critical die dimension requirements on Die #1 and #2 with simple dicing procedure.**

Reticle stepping increments with these rules are: 14.838 (W) x 15.378 (L) mm.



GDS of Reticle:



Next Steps for FE-I Design

Archive design:

- Collect all libraries, design kit, etc. and place together in small number of directories. The intention is to capture everything used for the submission in one area, to avoid private libraries, etc. This will allow us to make the next generations of the chips starting from the correct files.
- So far, have files for everything except MCC-I. Still continue to work on improving opto-chip schematics, which do not properly LVS with submitted designs.
- Will distribute CD-R version of files, arranged so that everything can be opened directly from the CD, in the next weeks. Extracted views being dropped, but all other views should be present.

Document front-end simulations:

- Many HSPICE simulations done of final 10fF and 5fF configurations, including parasitic capacitors and NWell diodes from layout.
- These cover threshold behavior, leakage behavior, TOT response, timewalk performance, double-pulse response, and cross-talk simulations.
- Still have to repeat threshold dispersion simulations for final design.
- This will be assembled into a “predicted performance” document, to allow comparison with actual performance in lab.

Complete TimeMill and PowerMill simulation program:

- Verification simulations done using complete digital column pair (320 pixels, 64 EOC buffers) and with complete small chip (16 pixels per column, 2 EOC buffers per column pair, all registers and control circuitry, all analog blocks).
- Typical simulations done for fully extracted netlists (small chip was 300K FETs and 330K caps !), but these were slow to run. More complete corner analysis done for schematic level netlists, with column bus parasitics added by hand.
- Simulations of worst case used VDD=1.8V, -3σ parameters, and 50MHz clock. Simple test vectors simulated correctly. Column pair stopped working under worst-case conditions at about 65MHz, due to sense amplifiers failing to deliver data in time. Other purely digital blocks seem to have more margin.
- Power analysis also being performed. Only preliminary results are dicussed below, as emphasis up to now has been on worst case timing studies and not on typical power consumption.
- Basic digital consumption is dominated by the column pair, but also has contributions of about 4mA for the LVDS I/O (4 receivers and 2 drivers), 2mA from the bottom digital logic (state machines and clock generators for running the chip), and 4mA standing current for the 19 HitBus receivers used. The HitBus receivers can be disabled when they are not in use.

- Column pair power consumption is about 40% in the column itself, and 60% in the EOC buffers. EOC buffer is larger due to clocked state machine per buffer. Present estimates vary from about 3.5mA - 5mA per column pair depending on whether the column pair is idle, or processing hits at a rate of 4MHz (similar to design luminosity occupancy of about 1 hit per crossing per chip).
- This suggests that FE-I1 will have an idle VDD consumption of about 35-40mA and an increased consumption of about 50mA when processing hits at design luminosity. Nominal budget was 25mA typical and 40mA worst case.
- Also studying current transients and role of internal decoupling capacitors in reducing/smoothing current spikes. Have given some preliminary numbers to Rusty for Flex studies. We see approximately 100mA/ns transient over a period of roughly 1-2ns near each clock edge. Some parts of FE-I use both clock edges, some use only leading edge, and others use a reduced frequency clock, so pattern is complex. Dynamic studies could guide Flex power distribution, as well as use of internal “smart” decoupling caps.
- Emphasize that these results are preliminary, and rely on a tool which we have never had a chance to compare with actual silicon, so we will refine our power analysis over the next months, and expect this tool to play a larger role in power optimization for FE-I2.
- Recommend that MCC-I team uses this tool to analyze their chip also. Beware that the standard cell library which we use has large annular devices, and individual DFF consume significant current and can generate large transients.

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Begin design work for improved front-end for FE-I2:

- Major concern for design included in FE-I1 is the large threshold dispersion, and the fact that the threshold seems to vary with irradiation. More minor concern is improvement of timewalk. Real measurements may bring to light further issues.
- Present schedule for FE-I2 is to submit another engineering run in Sept 02. This milestone is critical to overall pixel schedule, and will define when we finally begin fabricating production electronics wafers (nominally FE-I3).
- Meeting this milestone date suggests we should try to make another analog test chip in Mar 02 (just as this year), in order to develop an improved front-end design.
- Two possible prototyping paths, neither one is ideal. First is to participate in CERN MPW7 for 3-metal IBM, tentatively scheduled in mid-Mar 02. This requires major layout changes to adapt our design for only 3-metal (user survey by CERN indicated no interest in 5-metal MPW outside of ATLAS pixels). Second path is to submit to 5-metal TSMC 0.25μ through MOSIS, scheduled for Mar 11 02. This has advantage that layout is compatible with final chip, but there are many TSMC/IBM differences that affect optimizing analog design performance.
- We favor the TSMC path at this time, to avoid creating second set of layouts.
- Laurent is already thinking about how to modify/improve the threshold control and discriminator design, including re-considering AC-coupling.
- We will also invest modest effort in exploring a zero-crossing concept (this may never see silicon, depending on how the design proceeds).